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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,237	09/03/2003	Katsuki Hazama	20433-00601-US1	4842

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CONNOLLY BOVE LODGE & HUTZ LLP
SUITE 800
1990 M STREET NW
WASHINGTON, DC 20036-3425

EXAMINER	
WILCZEWSKI, MARY A	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,237	HAZAMA, KATSUKI	
	Examiner	Art Unit	
	Mary Wilczewski	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *68-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *68-79,81 and 82* is/are rejected.

7)☒ Claim(s) *80* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/720,014.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/09/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 68-74 and 76 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 76 recites that the lamination of the second conductive film and the first conductive film is patterned "in an element isolation region of said semiconductor substrate", see lines 4 and 5 of claim 76. However, as is shown in Figures 1H and 2B and disclosed in Applicant's specification on page 15, in lines 10-26, the lamination of the second and first conductive films is patterned in the peripheral circuit region of the substrate, not in the element isolation region. Likewise in claim 68, in lines 13-14, it is disclosed that the second insulating film is formed on the first conductive film in the active region *but not in an element isolation region*. As shown in Figure 1F and disclosed on page 14 of Applicant's specification, in lines 1-5, the second insulating film is not formed in the *peripheral circuit region* of the substrate. Although the peripheral circuit region does include isolation regions 2, it also includes an active region 4, hence claim 68 should be amended to recite that the second insulating film is formed "above at least said active region except for a peripheral circuit region", thereby precluding formation of the second insulating film on active region 4.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 75, 79, 81, and 82 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Usami et al., U.S. Patent 4,597,159.

Usami et al. disclose a method of manufacturing a semiconductor device having a floating gate in which a first insulating film 23 is formed on the surface of a semiconductor substrate 21 (Figure 3A); a first conductive film 24 is formed over the entire surface of the substrate (Figure 3A), an impurity is ion implanted into the first conductive film at a concentration of 5×10^{20} to 7×10^{20} atoms/cm^3 (Figure 3C and column 4, lines 32-36); a second insulating film 26 is then formed on the first conductive film (Figure 3E); a second conductive film 27 is formed over the entire surface of the substrate (Figure 3F); an impurity is thermally diffused into the second conductive at a concentration of 4×10^{20} to 6×10^{20} atoms/cm^3 (Figure 3F); and the lamination of layers is patterned into the shape of a single gate structure for a transistor (Figures 3G-3I and column 4, lines 52-59). Note that within the disclosed ranges of impurity concentrations, concentrations can be selected which would provide a higher doping concentration in the second conductive film than in the first conductive film.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 68-71, 73, 74, and 76-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami et al., U.S. Patent 4,597,159, in view of Hisanobu et al., JP 7-183411, cited by Applicant.

Usami et al. is applied as above. Usami et al. lack anticipation of forming the second insulating film comprising a multiplayer film including an oxide film and a nitride film in a memory cell region but not in a peripheral region and of patterning the lamination of the second and first conductive layers in the peripheral circuit region. Hisanobu et al. disclose a method of fabricating a memory device in which a multiplayer insulating film comprising oxide and nitride is used as an interelectrode insulating film and formed only in a memory cell region of the substrate, see figures 1(a)-1(f). Hisanobu et al. also disclose that the first conductive film 24 and the second conductive film 31 are patterned to form a control gate in a peripheral circuit region of the substrate in order to simplify processing (eliminating etching steps for the removal of first and second conductive films in the peripheral circuit region) and reducing the difference in height between gate structures formed in the memory cell region of the substrate and those formed in the peripheral circuit region of the substrate, see the English-language abstract. Therefore, in light of the teachings of Hisanobu et al. it

would have been obvious to one skilled in the art to form the second insulating film only in region of the substrate where memory devices are to be formed and to deposit and pattern the first and second conductive films to form control gates in the peripheral circuit region of the substrate, thereby simplifying the overall manufacturing process and to minimize height differences on the surface of the substrate.

Allowable Subject Matter

Claim 80 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 72 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited prior art, some of which has been cited in earlier-filed divisional applications, disclose various methods of fabricating memory devices having floating gates.

Any inquiry concerning this communication should be directed to M. Wilczewski at telephone number (571) 272-1849.

M. Wilczewski
Primary Examiner
Tech Center 2800